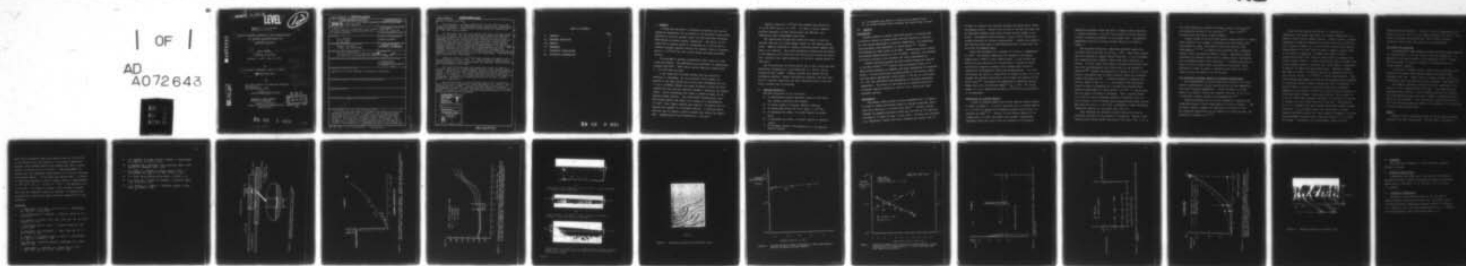
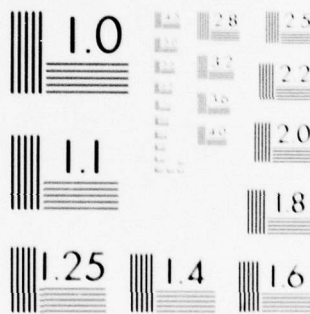


AD-A072 643 CORNELL UNIV ITHACA N Y SCHOOL OF ELECTRICAL ENGINEERING F/6 20/12
ELECTRIC-CURRENT CONTROLLED LIQUID PHASE EPITAXY OF COMPOUND SE--ETC(U)
1979 L F EASTMAN, C E WOOD, B VAN REES AFOSR-76-2929
UNCLASSIFIED AFOSR-TR-79-0913 NL

1 OF 1
AD
A072 643



END
DATE
FILMED
9-79
DOC



MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

18 AFOSR-TR- 79-0913

LEVEL II

12

Approved for public release;
distribution unlimited.

ELECTRIC-CURRENT CONTROLLED LIQUID PHASE EPITAXY
OF COMPOUND SEMICONDUCTORS FOR
MICROWAVE DEVICES

9 Final Report, 1 Oct 78 - 31 May 79,

Covering the Period

October 1, 1978 - May 31, 1979

by

10 Lester F./Eastman, Colin E.C./Wood
~~and~~ Bart/Van Rees

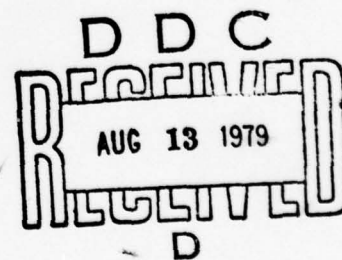
for

Air Force Office of Scientific Research
Building 410
Bolling AFB DC 20332

15 Contract No. AFOSR-76-2929

Approved for public release;
distribution unlimited.

Cornell University
School of Electrical Engineering
Phillips Hall



79 08 9 021

098 850

JOB

A072643

DDC FILE COPY

Unclassified
SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER AFOSR-TR- 79 - 09 13	2. GOVT ACCESSION NO.	3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle) Electric-Current Controlled Liquid Phase Epitaxy of Compound Semiconductors for Microwave Devices		5. TYPE OF REPORT & PERIOD COVERED Final Report 10/1/78 - 5/31/79
		6. PERFORMING ORG. REPORT NUMBER
7. AUTHOR(s) L.F. Eastman C.E.C. Wood B. Van Rees		8. CONTRACT OR GRANT NUMBER(s) AFOSR-76-2929 ⁴⁴
9. PERFORMING ORGANIZATION NAME AND ADDRESS Cornell University Ithaca, New York 14853		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS 61102F, 2306/B1
11. CONTROLLING OFFICE NAME AND ADDRESS Air Force Office of Scientific Res, <i>NE</i> Building 410, Bolling AFB, DC 20332		12. REPORT DATE 1979
		13. NUMBER OF PAGES 22
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office)		15. SECURITY CLASS. (of this report) UNCLASSIFIED
		15a. DECLASSIFICATION/DOWNGRADING SCHEDULE N/A
16. DISTRIBUTION STATEMENT (of this Report) Approved for Public Release: Distribution Unlimited		
17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)		
18. SUPPLEMENTARY NOTES		
19. KEY WORDS (Continue on reverse side if necessary and identify by block number)		
20. ABSTRACT (Continue on reverse side if necessary and identify by block number) → A study has been made to determine the growth rate and the mechanism responsible for the growth of InP epitaxial layers while applying an electric current across the melt-substrate interface, maintaining a constant overall temperature. The object of the study was to produce layers of thicknesses up to 100 μ m with a constant residual impurity profile for impurity levels of approximately $2 \times 10^{15}/\text{cm}^3$ for use in Gunn diodes and <i>10 to the 15th cu cm</i>		

~~UNCLASSIFIED~~

other microwave devices.

We succeeded in growing reproducibly thick layers of n-InP using this method. The experiments were performed at temperatures ranging from 630°C - 680°C while current densities ranging from 0 - 50 A/cm² were utilized.

It was found that the exact growth rate was relatively difficult to determine, for the so-called "Pulse method" as applied to the GaAs system did not yield any information for InP n⁻ melts. Probably because the etches available (Potassium ferrocyanide and A-B) were not sensitive enough to delineate the current spikes. Layer thicknesses were found to depend strongly on the applied current density. The relationship between growth rate and current density was found to be linear up to approximately 10 A/cm². When larger currents were applied, the growth rate increased very rapidly in a nonlinear fashion. A floating source seed was used to assure a constant growth rate during the experiment. Maximum growth rate obtained was $\approx 240 \mu\text{m/hr}$.

Impurity levels of $4.10^{15}/\text{cm}^3$ were reached with mobilities of 26,000 cm²/V-sec (at T = 77°K). In order to obtain impurity profiles Secondary Ion Mass Spectroscopy was employed, and differential Hall measurements were taken.

The capacitance-voltage plot method was found to yield unreliable data due to a high leakage current at the reverse biased diode. Impurity profiles at current controlled growth samples were found to be constant. The actual mechanism of growth was attributed to the migration of P-atoms with the electron flow toward the interface, creating local super-saturation of the melt causing growth to take place.

The contributions of Peltier-effect and of melt convection were effectively eliminated by using substrates of $< 350 \mu\text{m}$, and by varying the melt height. Surface textures were smooth and the thicknesses uniform. Slight terracing was observed, and was attributed to residual convection and small misorientations at the substrate surfaces due to polishing.

Accession For	
NTIS GRA&I	<input checked="checked" type="checkbox"/>
DDC TAB	<input type="checkbox"/>
Unannounced	<input type="checkbox"/>
Justification	
By _____	
Distribution/ _____	
Availability Codes	
Dist	Avail and/or special
A	

UNCLASSIFIED

TABLE OF CONTENTS

	PAGE
I. ABSTRACT	1
II. RESEARCH OBJECTIVES	2
III. RESULTS	3
IV. PERSONNEL	22
V. SCIENTIFIC PUBLICATIONS	22
VI. SCIENTIFIC INTERACTIONS	22

79 08 9 021

I. ABSTRACT

A study has been made to determine the growth rate and the mechanism responsible for the growth of InP epitaxial layers while applying an electric current across the melt-substrate interface, maintaining a constant overall temperature. The object of the study was to produce layers of thicknesses up to 100 μm with a constant residual impurity profile for impurity levels of approximately $2 \times 10^{15}/\text{cm}^3$ for use in Gunn diodes and other microwave devices.

We succeeded in growing reproducibly thick layers of n-InP using this method. The experiments were performed at temperatures ranging from 630°C - 680°C while current densities ranging from 0 - 50 A/cm^2 were utilized.

It was found that the exact growth rate was relatively difficult to determine, for the so-called "Pulse method" as applied to the GaAs system did not yield any information for InP n⁻ melts. Probably because the etches available (Potassium ferrocyanide and A-B) were not sensitive enough to delineate the current spikes. Layer thicknesses were found to depend strongly on the applied current density. The relationship between growth rate and current density was found to be linear up to approximately 10 A/cm^2 . When larger currents were applied, the growth rate increased very rapidly in a nonlinear fashion. A floating source seed was used to assure a constant growth rate during the experiment. Maximum growth rate obtained was $\approx 240 \mu\text{m}/\text{hr}$.

Impurity levels of $4.10^{15}/\text{cm}^3$ were reached with mobilities of $26,000 \text{ cm}^2/\text{V-sec}$ (at $T = 77^\circ\text{K}$). In order to obtain impurity profiles Secondary Ion Mass Spectroscopy was employed, and differential Hall measurements were taken.

The capacitance-voltage plot method was found to yield unreliable data due to a high leakage current at the reverse biased diode. Impurity profiles at current controlled growth samples were found to be constant. The actual mechanism of growth was attributed to the migration of P-atoms with the electron flow toward the interface, creating local super-saturation of the melt causing growth to take place.

The contributions of Peltier-effect and of melt convection were effectively eliminated by using substrates of $< 350 \text{ }\mu\text{m}$, and by varying the melt height. Surface textures were smooth and the thicknesses uniform. Slight terracing was observed, and was attributed to residual convection and small misorientations at the substrate surfaces due to polishing.

II. Research Objectives

The main objectives of the study were:

- a) To reproducibly produce epitaxial layers of InP using the "current controlled LPE" method.
- b) To obtain layers of constant impurity profiles.
- c) To obtain high purity InP of at most $5 \times 10^{15}/\text{cm}^3$.
- d) To determine the effect of current density on growth rates.
- e) To determine the effect of current density on impurity levels.
- f) To determine whether electromigration is the dominant cause of growth.

- g) To determine the effect of convection on growth rates.
- h) To obtain uniform layer thickness and smooth layer surface.

III. RESULTS

Introduction

Current induced or current controlled growth is obtained when an electric current is passed across the melt-substrate interface in a LPE system maintained at constant temperature. Two mechanisms have previously been identified to induce growth.⁽¹⁾ Firstly, electromigration takes place in the melt, transporting solute toward and causing supersaturation at the interface. Secondly, the presence of Peltier cooling at the interface can cause supersaturation.

Current controlled growth has been studied extensively applied to the GaAs-system,^(2,3,4) however some controversy exists as to which growth mechanism is dominant and hence responsible for observed growth. We have practically excluded growth by the Peltier effect, and have grown reproducibly thick layers ($\approx 100 \mu\text{m}$) of n-InP using C.C. LPE, and identified electromigration as the major mechanism responsible. The object of the study was to produce layers with a constant impurity profile for use in L.S.A. diodes and other microwave devices.

Experimental

The present growth system is shown diagrammatically in Figure 1. In order to reduce the Peltier effect at the melt substrate interface thin substrates (≈ 15 mils) were used.⁽⁵⁾ Electric contact between the graphite substrate holder and the back of the substrate was made by a liquid In layer ~ 5 mils thick. The melt was contained in a "Spectrosil" quartz boat which confined the current flow to

the melt by acting as an insulator between the electrically conducting graphite parts. Contact with the top of the melt was made with an adjustable graphite plug which allowed the melt height to be varied. The graphite plug contained a source crystal which maintained saturation of the melt during growth. Current was carried to and from the growth melt by Molybdenum-pushrods in electrical contact with the graphite parts.

Melts were prebaked for a minimum of 24 hrs at a temperature of 750°C . The furnace temperature was dropped to the growth temperature of 680°C 2 hours before growth. A pure In melt was moved over the substrate for 1 minute prior to growth in order to back etch substrate surfaces which became badly pitted by evaporation of Phosphorous during the prebake period. A 12 volt car-battery was used as a ripple free DC current source, as it was assumed that current fluctuations would effect the quality of the grown layer.⁽⁶⁾ Convection was suppressed by adjusting the melt height such that the Rayleigh number⁽⁷⁾ $N_{\text{Ra}} < 1700$. For a melt height of 1 cm a temperature gradient of $0.56^{\circ}\text{C}/\text{cm}$ was calculated to be admissable.

Growth Rate vs. Current Density

A plot of observed growth rate versus applied current density is shown in Figure 2. It can be seen that up to a current density of $\sim 10 \text{ A}/\text{cm}^2$ the growth rate increases linearly with current, as observed for GaAs^(2,4). However, as the current density is increased above $10 \text{ A}/\text{cm}^2$ the growth rate assumes a superlinear dependence which may result from the presence of a horizontal

temperature gradient across the melt at higher current densities. At current densities $> 10 \text{ A/cm}^2$ Joule heating of the Mo-pushrods creates a horizontal gradient in the furnace tube. The measured temperature profile at various current densities is shown in Figure 3.

The increased horizontal temperature gradient causes convective flow in the melt as now $N_{Ra} > 1700$. Since faster growth rates are observed at higher current densities, it can be assumed that enhanced solute transport takes place when convection is present. At first sight this seems at variance with earlier findings that electromigration only takes place in the absence of convection⁽⁸⁾ However the presence of a source on top of the melt allows a continuous flow of solute material toward the interface without depleting the melt. Thickness gradients along the substrates, shown in Fig. 4a, b, c, also support this explanation. Figure 4a shows a micrograph of a cleaved and potassium ferrocyanide stained edge of a layer grown at 5 A/cm^2 . It can be seen that the layer is uniform in thickness. When a current density of 10 A/cm^2 is used a thickness gradient is observed (Fig. 4b). This thickness gradient becomes more pronounced when higher current densities are applied ($\approx 38 \text{ A/cm}^2$), indicating a larger horizontal temperature gradient in the growth melt (Fig. 4c).

Some terracing was observed on grown layers which may be additional evidence of the presence of convection. However since terraced areas always border featureless flat areas (Fig. 5) it is

not clear whether the observed terracing is due to convection⁽⁶⁾ or orientation effects of the substrate.⁽⁹⁾ Recent work⁽¹⁰⁾ indicated that the latter is more probable.

Current pulses of 80 A/cm^2 were applied during growth at various time intervals in an attempt to determine the exact growth rate with respect to time. This method, previously used by other investigators,^(2,4,11) is based on the principle that a changing current alters incorporated impurity levels. Subsequent etching delineates the impurity spikes due to current pulses, and enables one to determine growth rates accurately. A suitable etch was not found for InP to expose these striations on n-epitaxial layers. Therefore in order to assure a constant growth rate with time a source crystal was added on top of the melt.

The Influence of Current Density on Impurity Concentration

Hall measurements on grown layers were carried out to obtain carrier concentrations ($N_D - N_A$) and mobilities at room temperature and liquid nitrogen temperature. A small increase in carrier density with applied current was observed (see Fig. 6), as is to be expected in growth caused by electromigration.⁽¹²⁾

Cumulative baking time of the melt appears to influence the background impurity levels significantly as shown in Figure 7. The principle impurity element was identified as silicon by SIMS. The mechanism responsible for the removal of Si from the melt was described by Eastman et al.⁽¹³⁾

Since the distributed coefficient is a function of temperature, and growth takes place at constant temperature, the impurity profile should remain constant. Figure 8 shows a constant background Si impurity concentration profile detected by SIMS and also reveals the effect of a 1 sec 80 A/cm^2 current pulse applied during growth at 10 A/cm^2 which produced a change in doping level of two orders of magnitude. Attempts were made to obtain capacitance-voltage plots from the grown layers to determine the carrier density profile. A metal-InP Schottky barrier suffers from a high leakage current in reversed bias, which makes it impossible to measure the depletion layer capacitance. Therefore attempts were made to obtain a rectifying junction by implanting the surface with Be (40 keV, $5 \times 10^{13}/\text{cm}^2$) to form p-type material. This method showed improvement in rectification characteristics compared to a Schottky barrier, however leakage was still considerable. A second attempt to obtain a rectifying diode was to evaporate Magnesium on the surface followed by a layer of gold to prevent an oxide layer from forming. After metallization a short anneal of 15 sec at 350°C under hydrogen atmosphere was required to allow Mg to diffuse into the surface and form p-type InP. Rectification up to 2.5 V reversed bias was obtained after which gradual leakage took place. This voltage however was insufficient to obtain adequate information about the carrier density throughout the layer since breakdown occurred after a depletion layer of 0.3 μm width was formed. Differential Hall-measurements showed constant

carrier profiles (Figure 9). Errors in the Hall-measurements are mainly due to the fact that the bromine-methanol etch tends to etch faster on surface non-uniformities, hence causing thickness variations which effect the outcome of the measurements.

The Effect of Tin-Doping

An unexpectedly large change in growth rate with current density was observed when 0.4% Sn was added to the melt (Figure 10). Sn migrates in the same direction of the electron flow.⁽¹⁴⁾ Hence, one would expect to observe a change in Sn-content when the current density changes.

In contrast to undoped layers, current pulse striations were observed on Sn-doped CCLPE samples showing that growth rates increased with time. Growth rates at currents above 5 A/cm^2 were sufficiently high that dendritic growth occurred. (See Figure 11).

The dramatic increase in growth rate can be explained if in some way a Sn-P complex forms in the melt. The large electron scattering cross section of such a complex molecule will enhance the electromigration drag force and a higher P concentration will result at the interface. Thus sufficiently large supersaturation will occur causing nucleation ahead of the interface, as is the case in constitutional supercooling.

Summary

Electric current controlled growth of InP on semi-insulating substrates has been investigated. We have shown it possible to

grow quality epitaxial layers with growth rates up to 200 $\mu\text{m/hr}$. It was observed that the presence of a horizontal temperature gradient could increase growth rates dramatically when a source crystal is present on top of the melt. SIMS measurements indicated that the background concentration of Si could be increased with current density. It was found that baking times $\gg 24$ hours at 750°C were necessary to obtain impurity levels of approximately $5 \times 10^{15} \text{ cm}^{-3}$ with $\mu_{77} = 26,000 \text{ cm}^2 \text{ V}^{-1} \text{ sec}^{-1}$. The addition of Sn to the melt (~ 0.4 atomic %) caused a rapid increase in growth rate such that dendritic growth was observed. We suspect that constitutional supercooling might have been responsible for this phenomenon.

References

1. L. Jastrzebski, H.C. Gatos, and A.F. Witt, J. Electrochem. Soc. 123, No. 7 (July 1976).
2. D.J. Lawrence and L.F. Eastman, J. Electron. Matls. 6, No. 1 (1977) p. 1.
3. J.J. Daniele, C. Michel, Inst. Phys. Conf. Ser. No. 24 (1975), Chapter 3, p. 155.
4. L. Jastrzebski and H.C. Gatos, J. Crystal Growth 42, (Dec. 1977) p. 309.
5. A. Abdul Fadl, E.K. Stefanakos, J. Appl. Phys. 47, No. 10 (Oct. 1976) p. 4627.
6. Y. Imamura, L. Jastrzebski and H.C. Gatos, J. Electrochem. Soc. 125, No. 9 (1978) p. 1560.
7. Lord Rayleigh, Scientific Papers 6, Cambridge Univ. Press (1920) p. 432.
8. L. Jastrzebski, J. Lagowski, H.C. Gatos and A.F. Witt, J. Appl. Phys. 49, No. 12 (Dec. 1978) p. 5909.

9. C.G. Baumann, R.W. Benz and M.H. Pilkuhn, J. Electrochem. Soc. 123, No. 8 (1976) p. 1232.
10. R. Messham and A. Majerfeld, 21st Electronic Matls. Conf. Session G-3, Boulder, Colo., 1979.
11. G.M. Blom, J.J. Daniele, T. Kyros, and A.F. Witt, J. Electrochem. Soc. 122, No. 11 (Nov. 1975) p. 1541.
12. V.B. Fiks, Soviet Physics-Solid State, 1 (1959) p. 14.
13. V.L. Wrick, K.T. Ip and L.F. Eastman, J. Electron. Matls. 7 No. 2 (1978) p. 253.
14. Y. K. Titova, S.I. Drakin, I. Balikina, Russian J. Phys. Chem. 42 (1968) p. 1194.

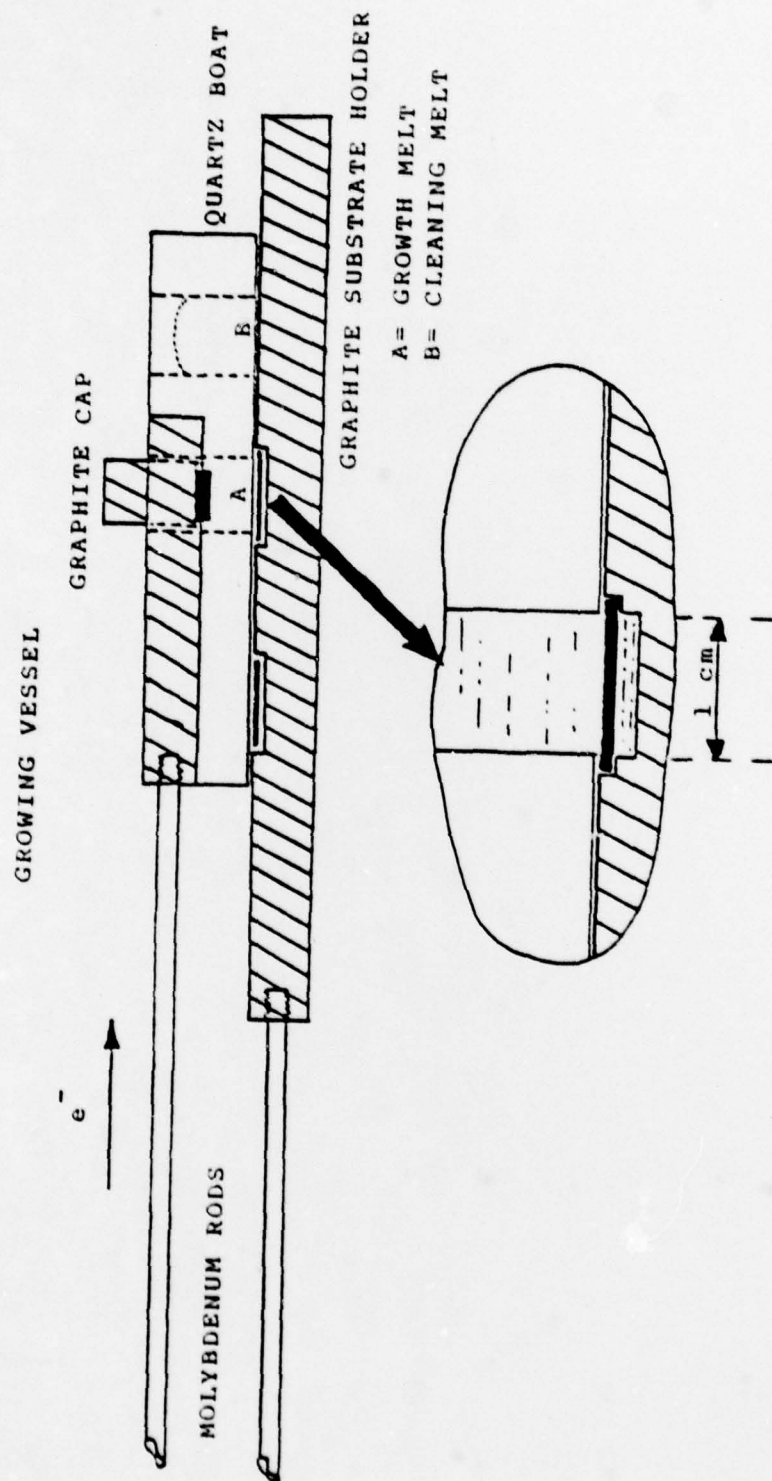


Figure 1. Diagrammatic representation of C.C.L.P.E. system.
(Cross-hatched areas indicate graphite parts).

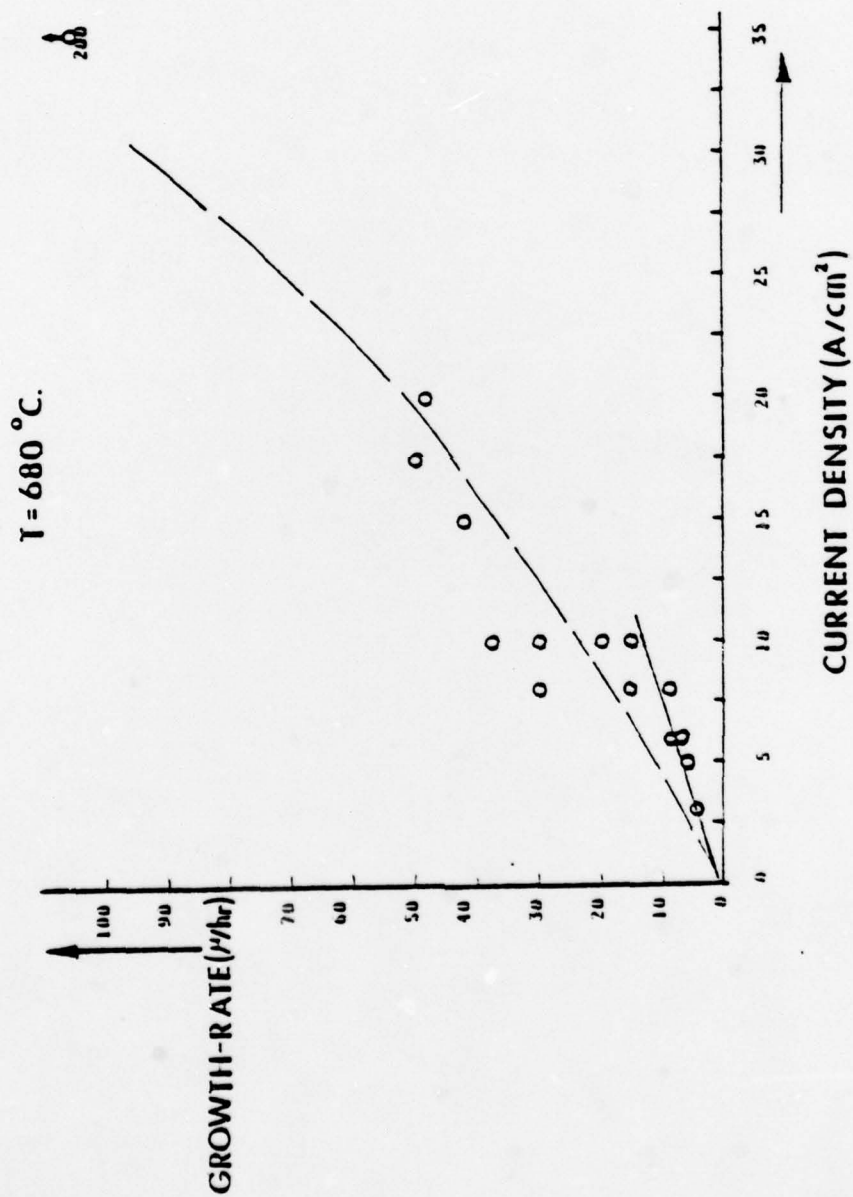


Figure 2. Plot of growth rate vs current density. (Solid line marks linear relationship. Dashed line shows superlinear dependence growth rate on current density).

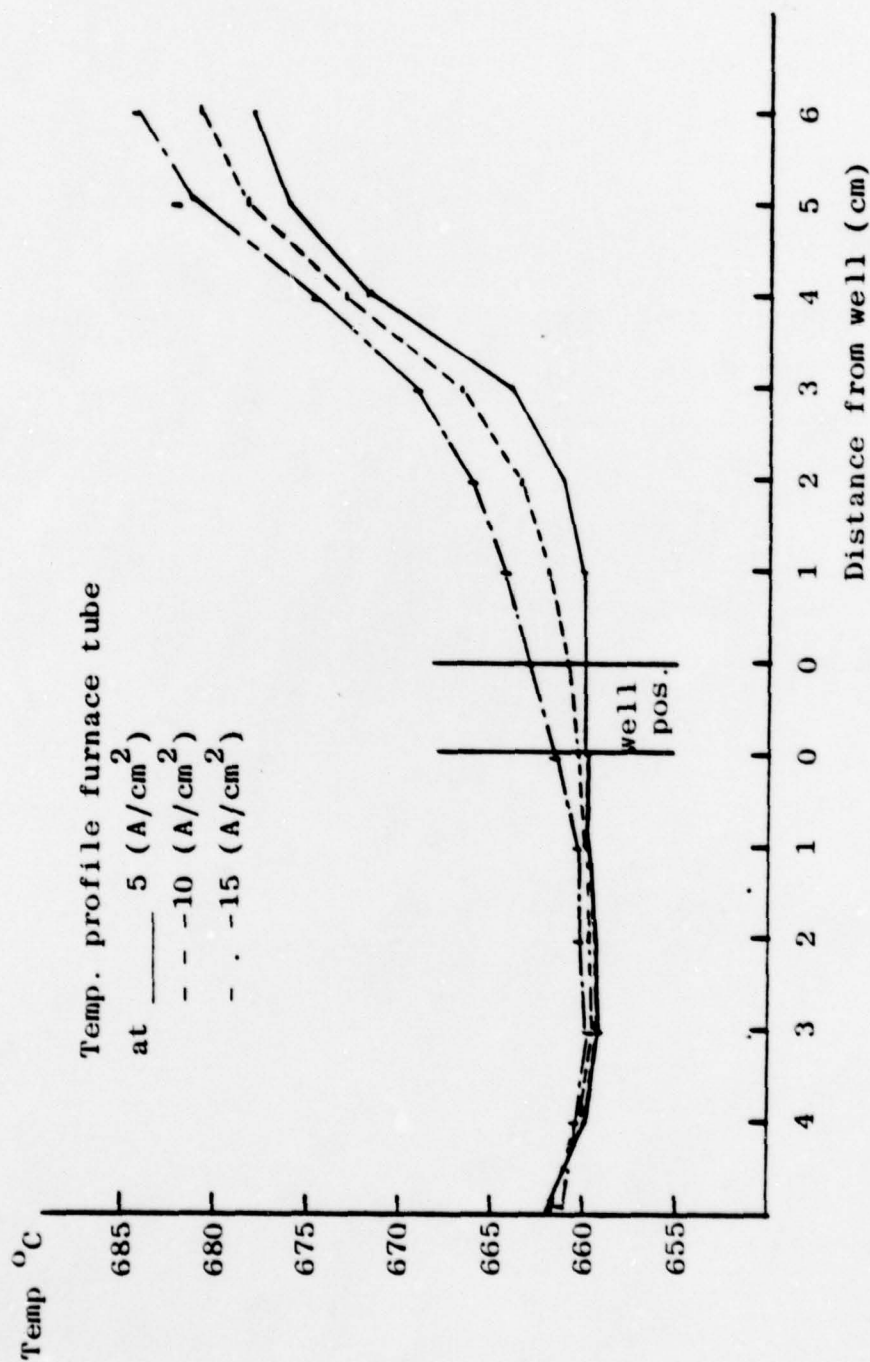


Figure 3. Temperature profile measured inside furnace tube at current densities of 5, 10, 15 A/cm^2 , showing increasing temperature gradient across melt at increasing current densities. (Solid vertical lines indicate well.)



(a)

8 mil thick layer grown in 1 hr at 5 A/cm^2 . Layer thickness is uniform across substrate.



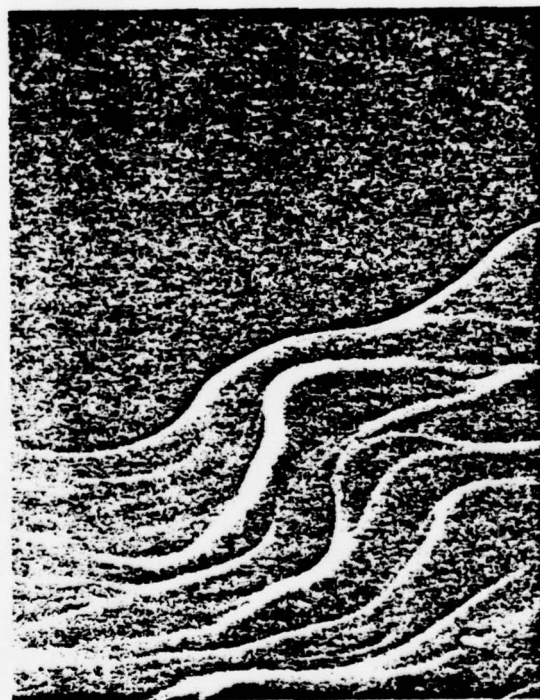
(b)

Layer grown at 10 A/cm^2 in 2 hrs. Thickness gradient is visible. Also note effect of etchback.



Layer grown at 38 A/cm^2 in 1 hr showing large thickness gradient. Dendrites on bottom of substrate grew from liquid electrode during rapid quench.

Figure 4.



(100 x)

Figure 5. Terracing observed on CCLPE grown layer.

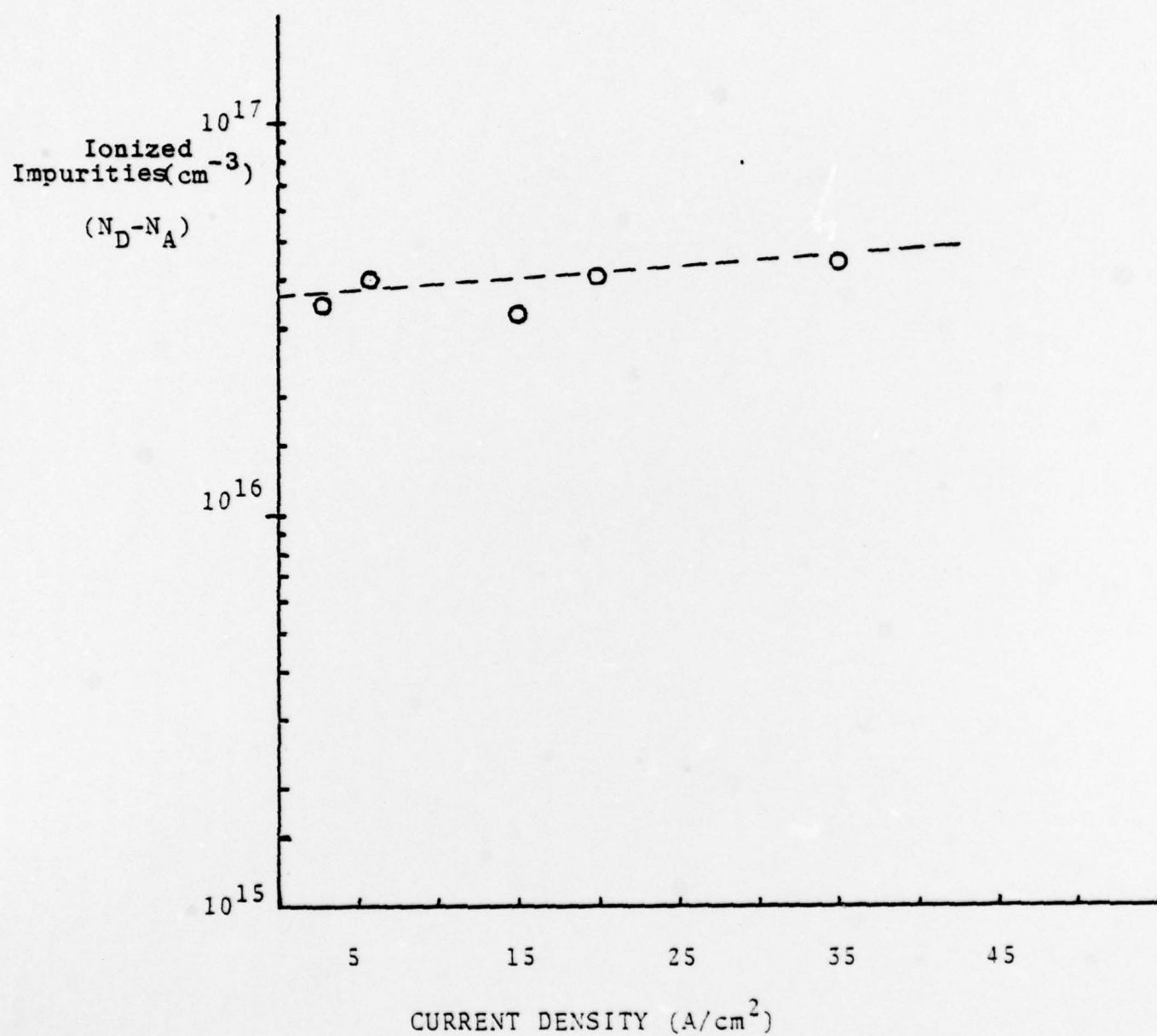


Figure 6. Ionized impurity levels determined by Hall measurements plotted vs applied current density.

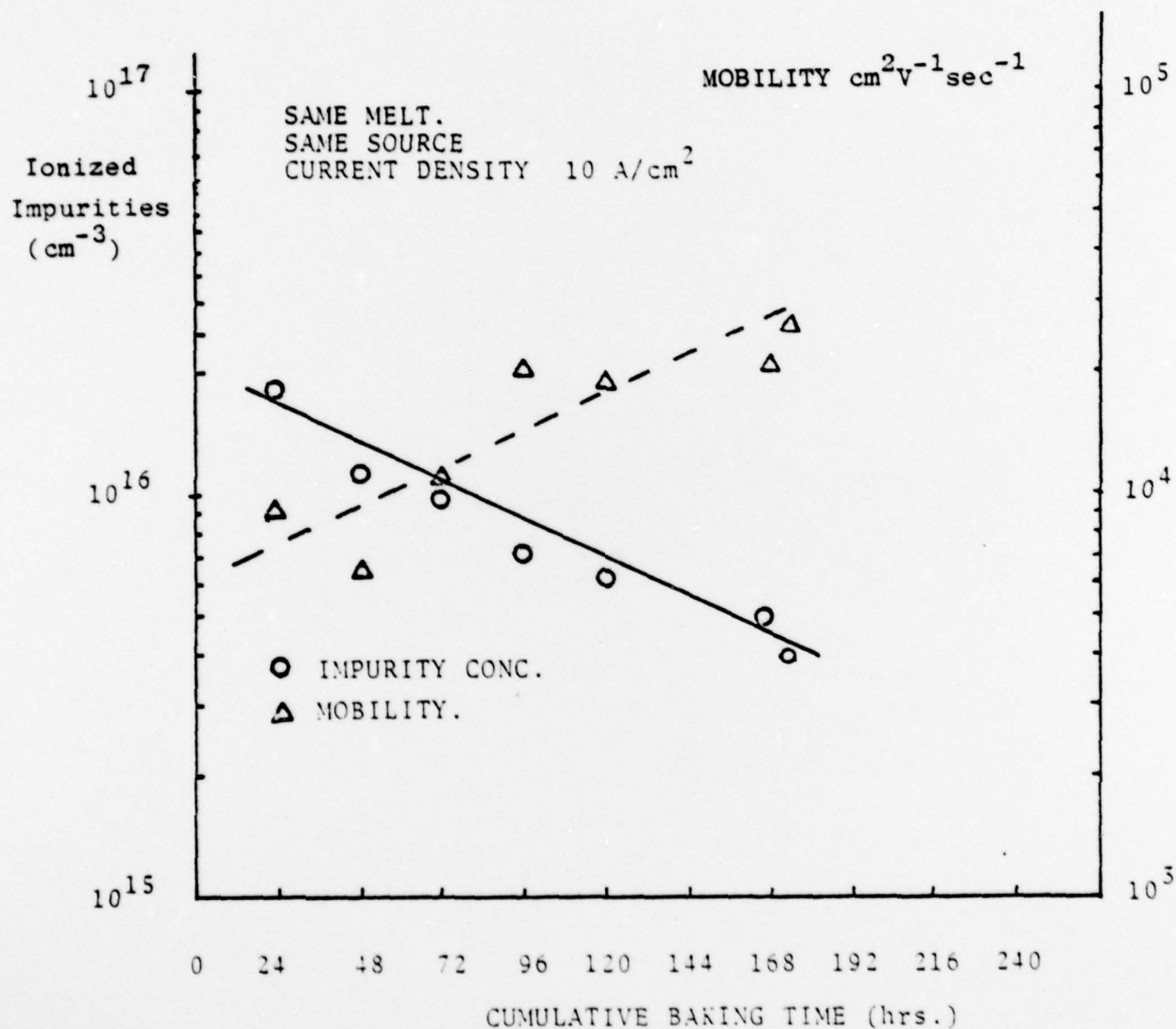


Figure 7. Cumulative baking time plotted vs ionized impurity levels and mobility of layers grown at 10 A/cm² from same melt with same source crystal.

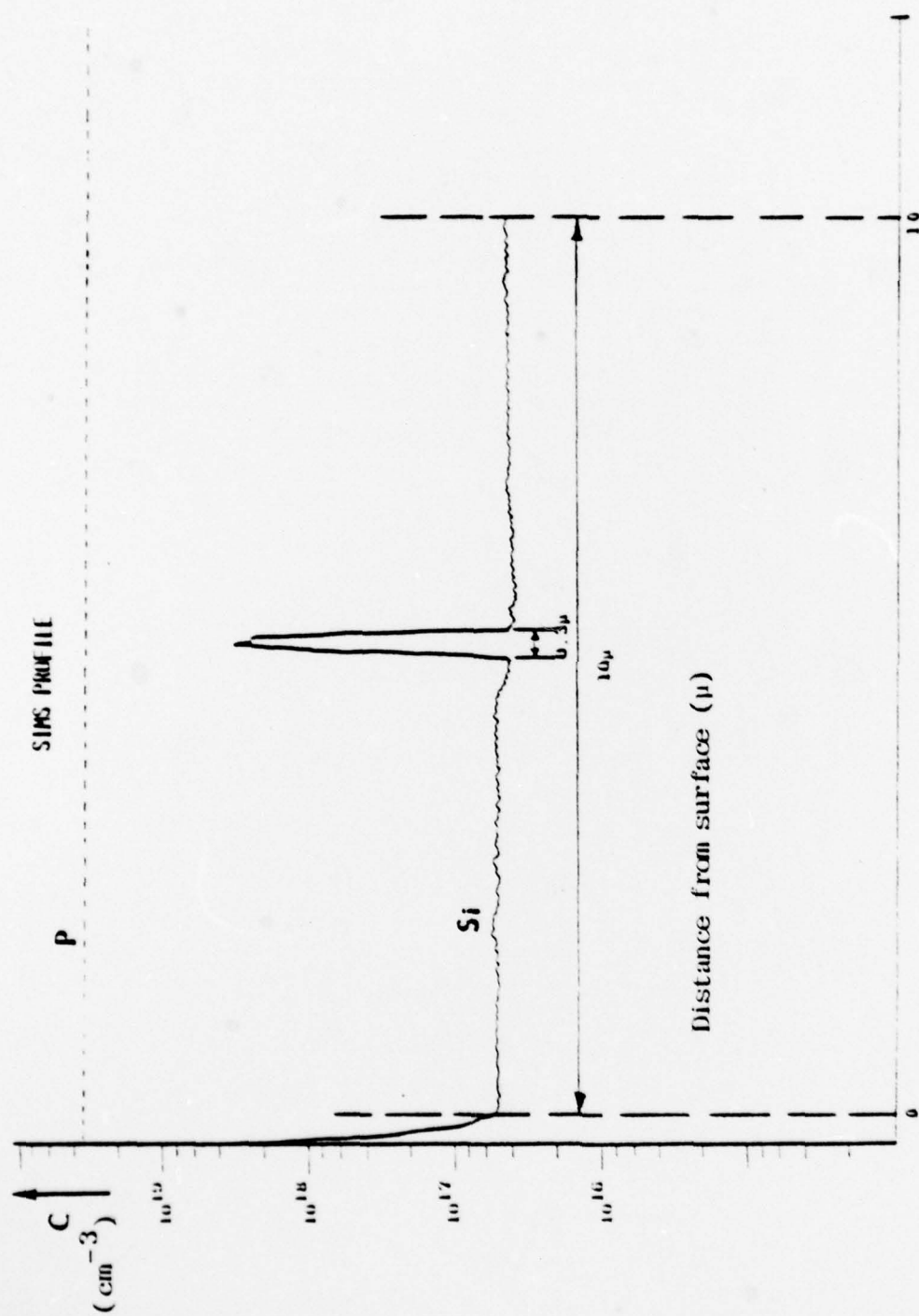


Figure 8. Si-profile determined by SIMS, showing effect of 80 A/cm^2 1 sec current pulse.

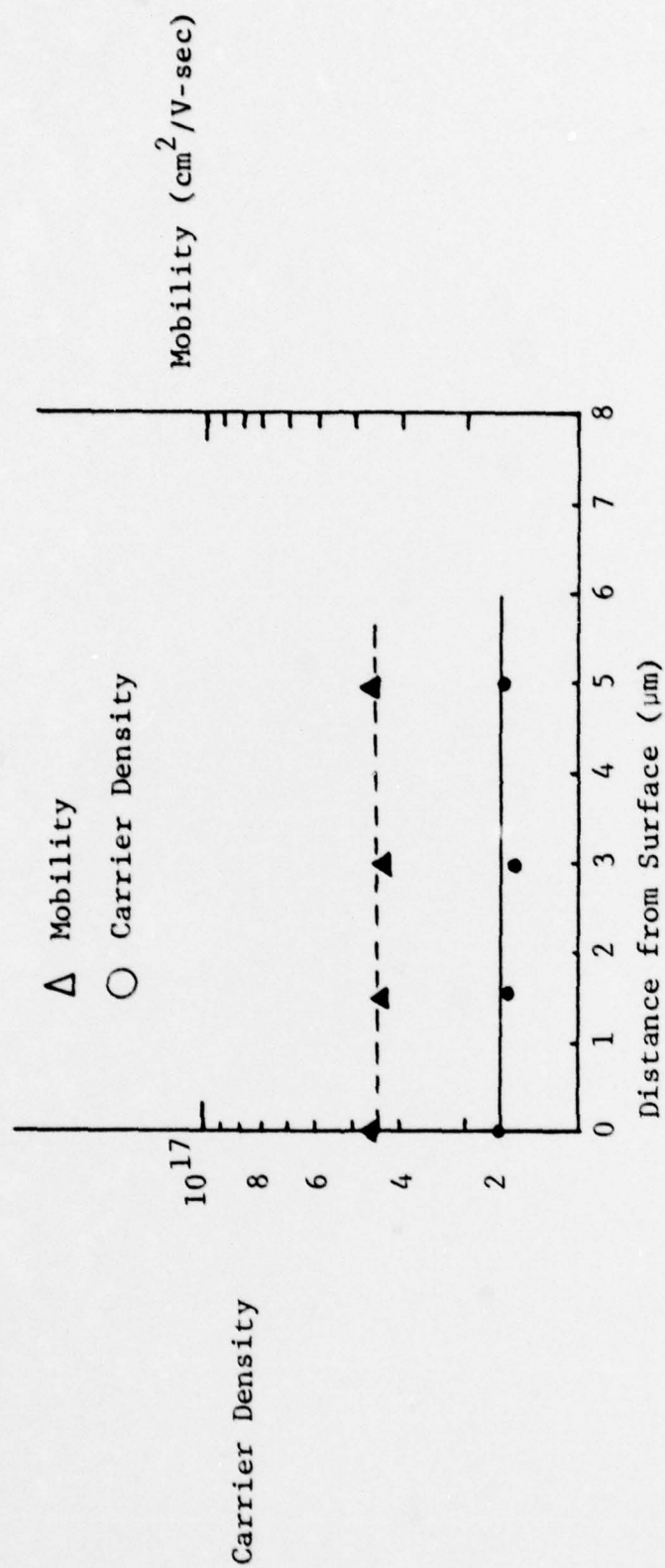


Figure 9. Ionized impurity levels and carrier mobilities plotted vs distance from surface.

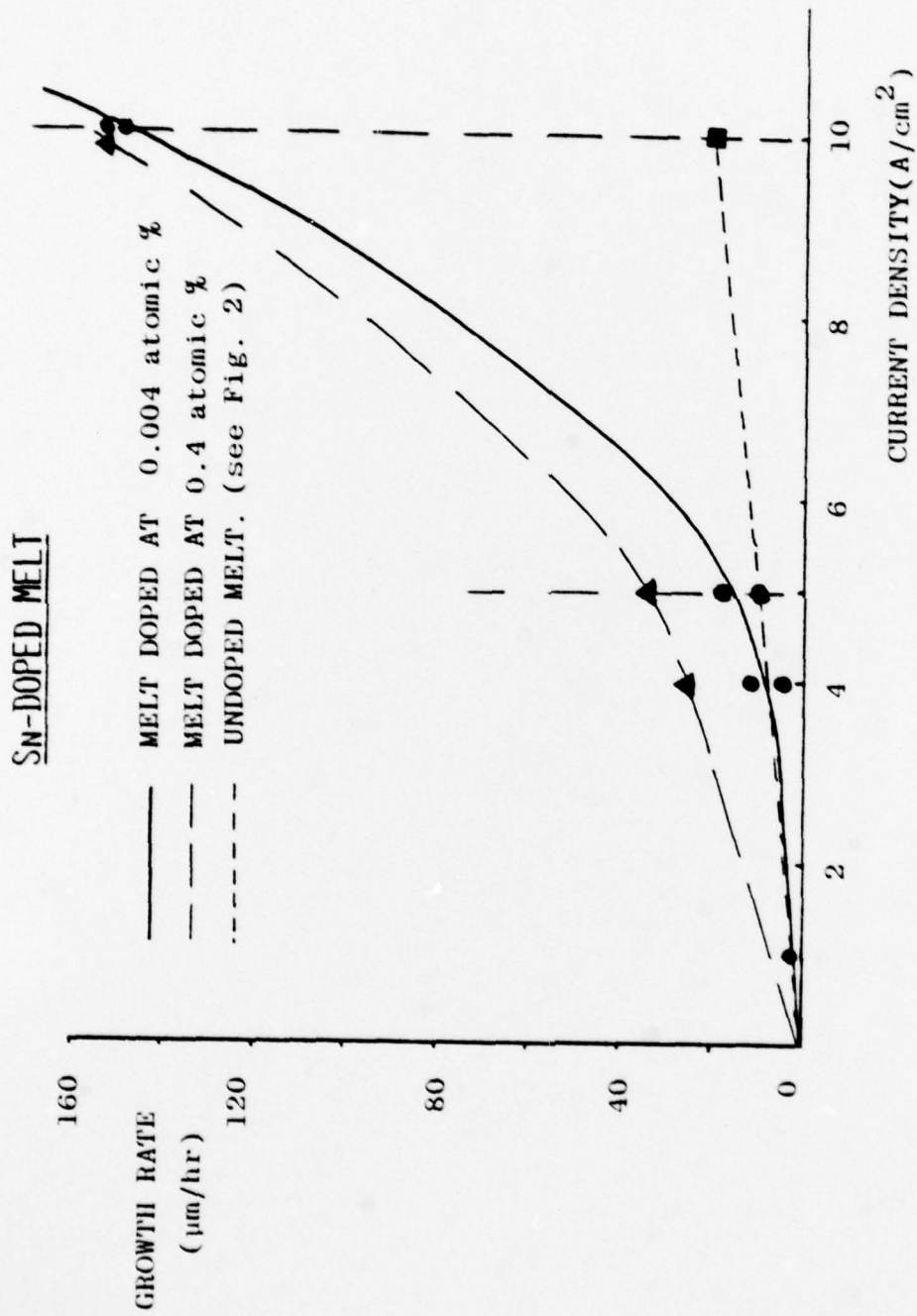


Figure 10. Plot of growth rate vs current density for Sn-doped melts. (Solid line indicates Sn-melt concentration of $10^{17} cm^{-3}$, dashed curve Sn-melt core of $10^{17} cm^{-3}$. Dotted line indicates undoped melt as in Figure 2.)

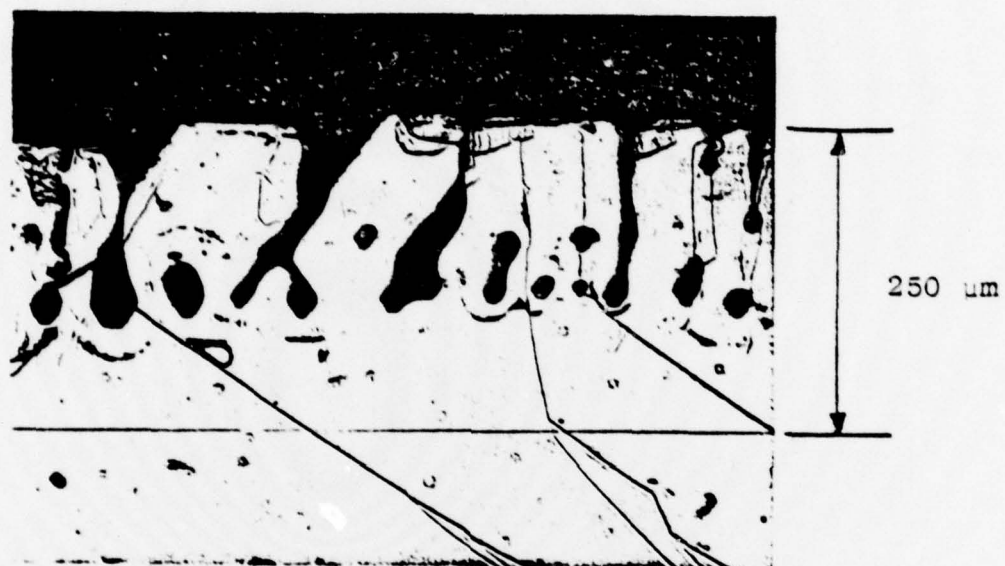


Figure 11. Dendrites formed on Sn-doped layer.

IV. PERSONNEL

This work was performed by H. Bart Van Rees, Graduate Research Assistant.

V. SCIENTIFIC PUBLICATIONS

A manuscript was submitted to the Journal of Electronic Materials entitled "Current Controlled LPE Growth of Microwave Device Quality InP-Layers" by B. Van Rees, C.E.C. Wood and L.F. Eastman.

VI. SCIENTIFIC INTERACTIONS

Lectures on this work were given by Mr. Van Rees at Hewlett-Packard Laboratories in Palo-Alto, California, and at the Western-Electric Engineering Research Center in Princeton, N.J. Results of this work were discussed with Dr. J.J. Daniele of Philips Research Labs at Briarcliff Manor, N.Y.

